ABSTRACT OF THE DISCLOSURE

A method for increasing integrated circuit density comprising stacking an upper wafer and a lower wafer, each of which have fabricated circuitry in specific areas on their respective face surfaces. The upper wafer is attached back-to-back with the lower wafer with a layer of adhesive applied over the back side of the lower wafer. The wafers are aligned so as to bring complimentary circuitry on each of the wafers into perpendicular alignment. The adhered wafer pair is then itself attached to an adhesive film to immobilize the wafer during dicing. The adhered wafer pair may be diced into individual die pairs or wafer portions containing more than one die pair.

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